REMARKS

The claims are claims 1 to 9.

Claims 1, 5, 8 and 9 are amended. Claims 1, 5, 8 and 9 are amended responsive to the Examiner's objection to informalities.

In claims 1 and 5 the term "image pixels" has been changed to "pixels" throughout. This change avoids confusion between the "image" of "image pixels" and the other recitations of "image."

The recitation of the limitation upon the dividing step of claim 1 has been amended as requested by the Examiner for clarity. The current language recites "each tile composed of a first predetermined number of pixels adjacently disposed in each scan line of a second predetermined number of adjacent scan lines." This recitation of the limitation is believed clear and properly reflective of the disclosure of this application as illustrated in Figure 3.

The requested amendment to claim 1, line 9 has been made according to the Examiner's suggestion.

The requested amendment to claim 1, line 12 suggested by the Examiner has not been made. Instead the recitation "an image" ahs been changed to "the image" referring to the image recited in the dividing step. The Applicant respectfully submits that the dividing step divides the image into tiles. The suggestion of the Examiner regarding line 12 would make the image the same as the tiles. The Applicant believes this is incorrect and would render the claim confusing.

Claims 8 and 9 have been amended as suggested by the Examiner.

Claims 1, 2, 4 to 6, 8 and 9 were rejected under 35 U.S.C. 102(e) as being anticipated by Chowdhuri et al.

Claims 1 and 5 recite subject matter not anticipated by Chowdhuri et al. Claim 1 recites "storing image data in a memory having data words of a predetermined data width, each data word

including said first predetermined number of pixels adjacently disposed in a single scan line, a set of said second predetermined number of consecutive data words corresponding to a two dimensional tile of the image whereby adjacent data words include pixels of adjacent scan lines." Claim 5 similarly recites "a memory storing image data having data words of a predetermined data width, each data word including a first predetermined number of pixels adjacently disposed on a single scan line, a set of a second predetermined number of consecutive data words corresponding to a two dimensional tile of said first predetermined number of pixels and said second predetermined number of scan lines of an image whereby adjacent data words include pixels of adjacent scan lines." These recitations differ from the disclosure of Chowdhuri et al.

This language of claims 1 and 5 require the data to be stored in the memory in tiles. This recitation is contrary to the teachings of Chowdhuri et al. Chowdhuri et al states at column 4, line 65 to column 5, line 2:

> "Pseudo tiling provides an impression to the graphics engine that the frame buffer is configured into a tile format, while, in reality, the cache memory, which is seen by the graphics engine, is configured into the tile format and the frame buffer is in scan line format. It should be understood that the term 'pseudo tile' is used when referring to the configuration of the pixel data stored in the frame buffer and the term 'tile' is used when referring to the configuration of the pixel data stored in the cache memory."

Chowdhuri et al states at column 6, lines 21 to 27:

> "It should be understood that the other system components are not affected by the addition of the tile cache 410A as they can still access the frame buffer 125 in standard data format (i.e., scan line format), meaning the other system components are not negatively affected as in the case of tiling the frame buffer itself."

Finally, Chowdhuri et al states at column 7, lines 30 to 32:

> "It should be understood that the frame buffer 125 stays in normal scan line order, but the tile cache 410A is in a tiled configuration."

Thus these portions of Chowdhuri et al clearly show that data is stored in SDRAM 120A in normal scan order and stored in tile cache 410A in tiles. This storage of data in normal scan order in SDRAM 120A is contrary to the above quoted portions of claims 1 and 5. Accordingly, claims 1 and 5 are not anticipated by Chowdhuri et al.

Claims 1 and 5 recite further subject matter not anticipated by Chowdhuri et al. Both claims 1 and 5 recite "each data word including said first predetermined number of pixels adjacently disposed in a single scan line." This limitation requires a single data word of the memory to store plural pixels. These plural pixels must be adjacent on a single scan line. Chowdhuri et al includes no teaching regarding the relative length of a data word and a pixel. Chowdhuri et al includes no teaching regarding data words at all. The Examiner's suggestion that the row disclosed in Chowdhuri et al corresponds to the recited data word finds no basis within the reference. Accordingly, claims 1 and 5 are not anticipated by Chowdhuri et al.

Claims 3 and 7 recite subject matter not made obvious by the combination of Chowdhuri et al and Mita et al. Claim 3 recites "said steps of transferring a tile of image data from the memory into the cache, performing image operations upon said tile of image data transferred to the cache, and transferring said tile of image data from the cache to the memory are performed by different data processors for different tiles." Claim 7 recites a second data processing apparatus and "wherein said data processing apparatus and said second data processing apparatus are programmed to operate

upon different tiles of image data simultaneously." Mita et al states at column 33, lines 51 to 64 (cited in the rejection):

> "FIG. 57 is a view showing the relationship among an input pixel block 591 corresponding to an original image 590, pixels 591a, a processor unit 592, processor elements 592a, and output image data 593a in an output image memory 593. In accordance with a control signal from a controller 594, the image data block 591 of 16 pertinent pixel elements in the original image memory 590 on the input side are accessed simultaneously, and the image data are accepted by respective ones of the processor elements 592a in the processor unit 562. The processor unit 592 computes typical density information 571 and detail information 572 such as shown in FIG. 55 from the 16 pixels of image data 591, and outputs the results to the image memory 593 on the output side."

This portion of Mita et al makes clear that pixel block 591 consists of pixels 591a. When pixel block 591 is accessed by processor unit 592, individual pixels 591a are processed by processor elements 592a. Thus a single tile (pixel block 591) is processed by a single processor (processor unit 592). Within the single tile are pixels 591a which are processed by processor elements 592a. Mita et al states at column 34, lines 45 to 60 (cited in the rejection):

> "By repeating the above-described processing through sequentially accessing the original image memory on the input side in 4X4 pixels block units until the compression processing for the final 4X4 pixels block of the original image memory is concluded, compression data equivalent to one page of the original image can be obtained.
>
> "In accordance with the present embodiment as described above, the raw data of the inputted original image, is sequentially accessed every memory block of mXn pixels (e.g. 44 pixels). Therefore, rather than accessing each pixel in the image memory on the input side a plurality of times, mXn pixels of image data can be accessed simultaneously. This makes it possible to transfer the image data while it is being compressed at high speed."

This portion of Mita et al clearly teaches repeated use of a single processing unit 592 to sequentially process pixel blocks 591 of the image 590. Note that processing elements 592a each process a single pixel 591a. This cannot be the tile recited in claims 3 and 7 which must include plural pixels. This fails to teach the use of plural processors to each process tiles as recited in claims 3 and 7. Accordingly, claims 3 and 7 are not made obvious by the combination of Maki et al and Mita et al.

The Applicants respectfully request entry and consideration of this amendment. Entry of this amendment is proper at this time because the amendment serves only to clarify subject matter previously recited. The only amendments made in this response were suggested by the Examiner in the FINAL REJECTION. Thus no new search or reconsideration is required.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early lentry of this amendment, reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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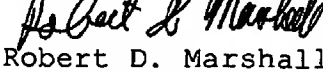
Respectfully submitted,



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